UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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			EXAMINER
23669	7590	12/15/2006	BRADLEY, MATTHEW A

HUFFMAN LAW GROUP, P.C.
1900 MESA AVE.
COLORADO SPRINGS, CO 80906

ART UNIT	PAPER NUMBER
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/766,784	DAVIES ET AL.
		Examiner	Art Unit
		Matthew Bradley	2187

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>03 October 2006</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49 and 52-71* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49,52-71* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

   1.☐ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action has been issued in response to amendment filed 3 October

2006. Applicant's arguments have been carefully and fully considered and are

persuasive. Therefore, the rejection has been withdrawn. However, upon further

consideration, a new ground(s) of rejection is made in view of Berry (U.S. 6,859,867).

Accordingly, this action has **NOT** been made final.

Claim Status

Claims 1-49 and 52-71 remain pending and are ready for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **1-8**, **10**, **24-27**, **29-34**, **39-49**, **52**, and **54-70** are rejected under 35

U.S.C. 102(e) as being anticipated by Berry (U.S. 6,859,867) hereinafter referred to as

Berry.

As per independent claim **1**, Berry teach,

- o A storage controller, comprising: a device interface adapter, for interfacing

  the storage controller to a plurality of logical storage devices; a host

interface adapter, for interfacing the storage controller to a plurality of host

computers; and a microprocessor, coupled to said device interface

adapter and host interface adapter, for processing requests to transfer

data between said plurality of logical storage devices and said plurality of

host computers; (Column 4 lines 1-21 as shown in Figure 2)

o wherein each of said requests specifies one of said plurality of host

computers and one of said plurality of logical storage devices for

transferring said data between, wherein said host interface adapter is

configured to receive said requests and to determine for each of said

requests whether the host computer identified in said request is allowed to

access the logical storage device identified in said request (Column 7 lines

14-22).

As per dependent claim **2**, Berry teach,

o The storage controller of claim 1, wherein if said host interface adapter

determines said host computer identified in said request is allowed to

access said logical storage device identified in said request, said host

interface adapter provides said request to said microprocessor, wherein

said microprocessor responsively controls said device interface adapter to

cause said device interface adapter to access said logical storage device

specified in said request to transfer said data between said logical storage

device and the storage controller (Column 6 lines 59-65).

As per dependent claim **3**, Berry teach,

o The storage controller of claim 1, wherein if said host interface adapter determines said host computer identified in said request is not allowed to access said logical storage device identified in said request, said host interface adapter transmits to said host computer a response indicating that said host computer identified in said request is not allowed to access said logical storage device identified in said request (Column 6 line 65 to Column 7 line 13).

As per dependent claim **4**, Berry teach,

o The storage controller of claim 1, wherein if said host interface adapter determines said host computer identified in said request is not allowed to access said logical storage device identified in said request, said host interface adapter provides to said microprocessor an indication that said host computer identified in said request is not allowed to access said logical storage device identified in said request (Column 6 line 65 to Column 7 line 13).

As per dependent claim **5**, Berry teach,

o The storage controller of claim 4, wherein said microprocessor causes said host interface adapter to transmit a response to said host computer identified in said request in response to said indication, wherein said response indicates said host computer is not allowed to access said logical storage device identified in said request (Column 6 line 65 to Column 7 line 13).

As per dependent claim **6**, Berry teach,

- o The storage controller of claim 1, wherein said host interface adapter is configured to interface said storage controller to said one or more host computers via an interface protocol (Column 4 lines 1-32).

As per dependent claim **7**, Berry teach,

- o The storage controller of claim 6, wherein said interface protocol comprises Fibre Channel (Column 3 lines 55-56).

As per dependent claim **8**, Berry teach,

- o The storage controller of claim 6, wherein said interface protocol comprises Small Computer Systems Interface (SCSI) (Column 3 lines 1-35).

As per dependent claim **10**, Berry teach,

- o The storage controller of claim 6, wherein said interface protocol comprises one of the following protocols: Infiniband, Ethernet, TCP/IP, HIPPI, Token Ring, Arcnet, FDDI, LocalTalk, ESCON, FICON, ATM, SAS, SATA, and combinations thereof (Column 3 line 55).

As per independent claim **24**, Berry teach,

- o A storage controller for providing hosts controlled access to logical storage devices, comprising: a memory, for storing an access table specifying which of the hosts has access to which of the logical storage devices; and (Column 5 lines 31-33)

- o an interface adapter, coupled to said memory, configured to interface the storage controller with a transport medium, receive on said transport medium from one of the hosts a request to access one of the logical storage devices, and determine from said access table whether said one of the hosts has access to said one of the logical storage devices (Column 4 lines 1-21 as shown in Figure 2 and Column 7 lines 14-22).

As per dependent claim **25**, Berry teach,

- o The storage controller of claim 24, wherein said interface adapter is configured to interface the storage controller with said transport medium according to a predetermined protocol (Column 3 lines 19-35).

As per dependent claim **26**, Berry teach,

- o The storage controller of claim 25, wherein said predetermined protocol comprises Fibre Channel (Column 3 lines 55-56).

As per dependent claim **27**, Berry teach,

- o The storage controller of claim 25, wherein said predetermined protocol comprises Small Computer Systems Interface (SCSI) (Column 3 lines 1-35).

As per dependent claim **29**, Berry teach,

- o The storage controller of claim 25, wherein said predetermined protocol comprises one of the following protocols: Infiniband, Ethernet, TCP/IP, HIPPI, Token Ring, Arcnet, FDDI, LocalTalk, ESCON, FICON, ATM, SAS, SATA, and combinations thereof (Column 3 line 55).

As per dependent claim **30**, Berry teach,

o The storage controller of claim 25, wherein said predetermined protocol comprises a low-level block protocol (Column 6 lines 59-65). *The Examiner notes that as the system of Berry allows the command to complete, or once access is granted, the system will access the data at a low-level on the drive associated with the physical devices.*

As per dependent claim **31** Berry teach,

o The storage controller of claim 24, further comprising: a microprocessor, coupled to said interface adapter, for programming said interface adapter to cause said interface adapter to transfer data on said transport medium (Column 3 lines 8-10).

As per dependent claim **32**, Berry teach,

o The storage controller of claim 31, wherein if said interface adapter determines that said one of the hosts has access to said one of the logical storage devices, said interface adapter provides said request to said microprocessor, and said microprocessor responsively processes said request to cause said one of the logical storage devices to be accessed (Column 6 lines 59-65).

As per dependent claim **33**, Berry teach,

o The storage controller of claim 31, wherein said microprocessor comprises a general purpose microprocessor (Column 3 lines 8-10).

As per dependent claim **34**, Berry teach,

o The storage controller of claim 31, wherein said microprocessor is distinct from said interface adapter (Column 3 lines 8-18). *The Examiner notes that as shown in Figure 2 and with respect to the citing, the instant microprocessor is distinct from the interface adapter.*

As per dependent claim **39**, Berry teach,

o The storage controller of claim 31, wherein said microprocessor does not include a direct memory access controller Column 3 lines 8-10).

As per dependent claim **40**, Berry teach,

o The storage controller of claim 31, further comprising: a storage device interface adapter, coupled to said microprocessor, configured to interface the storage controller with the logical storage devices (Column 3 lines 8-18).

As per dependent claim **41**, Berry teach,

o The storage controller of claim 40, wherein said microprocessor causes said storage device interface adapter to transfer data between the logical storage devices and the storage controller in response to said interface adapter providing said request to said microprocessor (Column 6 lines 59-65).

As per dependent claim **42**, Berry teach,

o The storage controller of claim 24, wherein said interface adapter comprises a single integrated circuit (Figure 2 shown as the IC between the instant devices compromising the adapter).

As per dependent claim **43**, Berry teach,

- The storage controller of claim 24, wherein said interface adapter comprises a set of integrated circuits specialized for performing a predetermined protocol on said transport medium (Figure 2 shown as the 'controllers'). *The Examiner notes that as shown in Figure 2, there exists multiple integrated circuits for which the adapter performs a protocol on over the transport medium.*

As per dependent claim **44**, Berry teach,

- The storage controller of claim 24, wherein the storage controller creates said access table in said memory in response to user input (Column 3 lines 8-18).

As per dependent claim **45**, Berry teach,

- The storage controller of claim 44, further comprising: a management controller, coupled to said memory, for creating said access table in response to user input (Column 3 lines 8-18).

As per dependent claim **46**, Berry teach,

- The storage controller of claim 24, wherein said interface adapter maps a first identifier to a second identifier, wherein said first identifier is included in said request and is used by the host to specify said one of the logical storage devices, wherein said second identifier is used by the storage controller to specify said one of the logical storage devices (Column 5 line 66 to Column 6 line 8).

As per dependent claim **47**, Berry teach,

- o   The storage controller of claim 46, wherein said interface adapter uses said second identifier to determine from said access table whether said one of the hosts has access to said one of the logical storage devices (Column 7 lines 14-42).

As per dependent claim **48**, Berry teach,

- o   The storage controller of claim 24, wherein said memory for storing said access table is comprised within said interface adapter (Figure 2 as shown with respect to item 222 and taught further in Column 5 lines 31-33).

As per dependent claim **49**, Berry teach,

- o   The storage controller of claim 24, wherein said memory for storing said access table is directly coupled to said interface adapter (Figure 2 shown as the interconnections between 220 and 222).

As per independent claim **52**, Berry teach,

- o   A method for controlling access by host computers to logical storage devices, the method comprising: performing a protocol to receive a request from a host computer to access a logical storage device; (Column 7 lines 14-22)

- o   determining whether the host computer has access to the logical storage device; and (Column 7 lines 14-22)

- o causing the logical storage device to transfer data, if the host computer
  has access to the logical storage device based on said determining;
  (Column 9 lines 59-65)

- o wherein said performing the protocol and said determining are performed
  by an interface adapter, and said causing the logical storage device to
  transfer the data is performed by a microprocessor distinct from the
  interface adapter (Column 3 liens 8-18).

As per independent claim **54**, Berry teach,

- o A storage controller for providing host computers access to storage
  devices, comprising: a microprocessor, for identifying each of the storage
  devices according to a unique internal identifier, and for processing
  requests to access the storage devices, each of said requests including a
  host identifier and an external identifier, said host identifier identifying one
  of the host computers making said request, and said external identifier
  identifying one of the storage devices to be accessed; and (Column 3
  lines 8-18)

- o a host interface adapter, coupled to said microprocessor, for receiving
  said requests from the host computers and mapping said external
  identifier received in said request to its said unique internal identifier
  based on said host identifier received in said request (Column 7 lines 14-
  22).

As per dependent claim **55**,Berry teach,

o   The storage controller of claim 54, further comprising: a mapping table,

accessible by said host interface adapter, for storing mapping information,

wherein said host interface adapter maps said external identifier received

in said request to its said unique internal identifier based on said host

identifier received in said request using said mapping information stored in

said mapping table (Column 5 lines 15-35).

As per dependent claim **56** Berry teach,

o   The storage controller of claim 55, wherein each unique combination of

host identifier and external identifier identifies a single one of the storage

devices according to a many-to-one mapping (Column 5 lines 15-35).

As per dependent claim **57**, Berry teach,

o   The storage controller of claim 54, wherein said host interface adapter

provides said unique internal identifier and said request to said

microprocessor for processing after said mapping said external identifier

to said unique internal identifier (Column 5 lines 15-35).

As per dependent claim **58**, Berry teach,

o   The storage controller of claim 54, wherein said host interface adapter is

further configured to perform a low-level protocol to interface the storage

controller with the host computers (Column 6 lines 59-65). *The Examiner

notes that as the system of Berry allows the command to complete, or

once access is granted, the system will access the data at a low-level on

the drive associated with the physical devices.*

As per dependent claim **59**, Berry teach,

   o   The storage controller of claim 54, wherein said unique internal identifier
       identifies a logical storage device, wherein said logical storage device
       comprises a grouping of physical storage devices (Column 5 lines 15-35).

As per dependent claim **60**, Berry teach,

   o   The storage controller of claim 54, wherein said unique internal identifier
       identifies a logical storage device, wherein said logical storage device
       comprises a portion of a grouping of physical storage devices (Column 5
       lines 15-35).

As per dependent claim **61**, Berry teach,

   o   The storage controller of claim 54, wherein said unique internal identifier
       identifies a logical storage device, wherein said logical storage device
       comprises a portion of a physical storage device (Column 5 lines 15-35).

As per dependent claim **62,** Berry teach,

   o   The storage controller of claim 54, wherein each of said requests specifies
       one of the storage devices in said external identifier in a protocol-specific
       manner (Column 5 lines 15-35).

As per dependent claim **63**, Berry teach,

   o   The storage controller of claim 62, wherein said protocol-specific manner
       comprises a SCSI logical unit number (Column 3 lines 1-35).

As per dependent claim **64**, Berry teach,

o   The storage controller of claim 54, wherein said external identifier

comprises a SCSI logical unit number (Column 3 lines 1-35).

As per dependent claim **65**, Berry teach,

o   The storage controller of claim 54, wherein said host interface adapter is

further configured to perform access control based on said unique internal

identifier and said host identifier (Column 5 lines 15-35).

As per independent claim **66**, Berry teach,

o   A method for mapping host-specific storage device identifiers to storage

controller-specific storage device identifiers, the method comprising:

receiving from a host computer a request to access one of a plurality of

storage devices coupled to a storage controller, the request specifying an

identifier of the host computer and an identifier of the one of the plurality of

storage devices, wherein said receiving is performed by a host interface

adapter of the storage controller; (Column 7 lines 14-22)

o   mapping a combination of the host computer identifier and the identifier of

the one of the plurality of storage devices to a unique identifier used by a

microprocessor of the storage controller to identify the one of the plurality

of storage devices, wherein said mapping is performed by the host

interface adapter; and (Column 5 lines 15-35)

o   providing the unique identifier to the microprocessor for processing the

request, wherein said providing is performed by the host interface adapter

(Column 7 lines 14-22).

As per independent claim **67**, Berry teach,

- o A storage controller, comprising: a first microprocessor, for processing

  requests from a host computer to access one of a first set of logical

  storage devices coupled to the storage controller; a second

  microprocessor, for processing requests from said host computer to

  access one of a second set of logical storage devices coupled to the

  storage controller; and (Figure 2 as taught in Column 3 lines 8-18). *The*

  Examiner notes that Berry teach multiple controllers thereby anticipating

  the instant limitation.

- o an interface adapter, coupled to said first and second microprocessors, for

  receiving said requests from said host computer, and for each of said

  requests determining whether said request specifies a logical storage

  device in said first set or said second set and providing said request to

  one of said first and second microprocessors based on said determining

  (Column 7 lines 14-22).

As per dependent claim **68**, Berry teach,

- o The storage controller of claim 67, wherein said first and second set of

  logical storage devices are distinct (Column 2 lines 52-59).

As per dependent claim **69**, Berry teach,

- o The storage controller of claim 67, wherein said first and second set of

  logical storage devices are programmable (Column 2 lines 52-59).

As per dependent claim **70**, Berry teach,

    o The storage controller of claim 67, wherein said first and second set of

logical storage devices are user-configurable (Column 2 lines 52-59).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed
> or described as set forth in section 102 of this title, if the differences between the
> subject matter sought to be patented and the prior art are such that the subject
> matter as a whole would have been obvious at the time the invention was made
> to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was
> made.

Claims **9** and **28** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Berry and in view of Camble et al (U.S. 6,999,999) hereinafter referred to as Camble.

As per dependent claim **9**, Berry teach the limitations as noted supra.

Berry does not explicitly teach the use of iSCSI.

Camble teach, the storage controller of claim 6, wherein said interface protocol

comprises Internet SCSI (iSCSI) (Column 7 lines 37-40).

Berry and Camble are analogous art because they are from the same field of

endeavor, namely computer storage systems.

At the time of invention it would have been obvious to one of ordinary skill in the

art, having both the teachings of Berry and Camble before him/her, to extend the

interfaces of Berry to encompass iSCSI systems for the benefit of increased

compatibility.

The motivation for doing so would have been that increased system capability allows for additional systems that the Berry system is employed upon. Increasing the number of interfacing standards also allows more flexibility when selecting the components to comprise the system.

Therefore, it would have been obvious to combine Berry with Camble for the benefit of increased capability to obtain the invention as specified in claims 9 and 28.

As per dependent claim **28**, the combination of Berry and Camble teach,

- o The storage controller of claim 25, wherein said predetermined protocol comprises Internet SCSI (iSCSI) (Column 7 lines 37-40 of Camble).

Claims **11-12, 35-38, 53,** and **71** are rejected under 35 U.S.C. 103(a) as being unpatentable over Berry and in view of Kitamura et al (U.S. 2002/0199071) hereinafter referred to as Kitamura.

As per dependent claim **11**, Berry teach the limitations as noted supra.

Berry does not explicitly teach the use of a buffer memory.

Kitamura teach, a buffer memory, coupled to said device interface adapter and said host interface adapter, for buffering data transferred between said plurality of host computers and said plurality of logical storage devices via said host interface adapter and said device interface adapter (Paragraph 0026). *The Examiner notes that the cache memory of Kitamura anticipates the instant limitation of buffer memory.*

Berry and Kitamura are analogous art because they are from the same field of endeavor, namely selectively allowing host computers to access storage devices.

At the time of invention it would have been obvious to one of even rudimentary

skill in the art, having both the teachings of Berry and Kitamura before him/her, to

integrate the cache memory of Kitamura into Berry for the benefit increasing the speed

of processing accesses from the host to the storage system.

The motivation for doing so would have been that, the cache memory stores data

frequently read from the disk or temporarily stores write data to be transferred from the

host or the like to the storage system to thereby increase the speed of processing

accesses from the host or the like (Paragraph 0026 of Kitamura).

Therefore, it would have been obvious to combine Berry with Kitamura for the

benefit of increased speed when processing accesses from the host to the storage

system to obtain the invention as specified in claims 11-12, 35-38, 53, and 71.

As per dependent claim **12**, the combination of Berry and Kitamura teach,

- o The storage controller of claim 11, wherein said microprocessor manages

    use of said buffer memory by said host interface adapter and said device

    interface adapter (Paragraph 0026 as shown in Figure 1 of Kitamura).

As per dependent claim **35**, the combination of Berry and Kitamura teach,

- o The storage controller of claim 31, further comprising: a buffer memory,

    coupled to said interface adapter, for buffering data transferred between

    the hosts and the logical storage devices (Paragraph 0026 as shown in

    Figure 1 of Kitamura).

As per dependent claim **36**, the combination of Berry and Kitamura teach,

   o   The storage controller of claim 35, wherein said microprocessor is configured to manage use of said buffer memory for buffering said data (Paragraph 0026 as shown in Figure 1 of Kitamura).

As per dependent claim **37**, the combination of Berry and Kitamura teach,

   o   The storage controller of claim 35, wherein said interface adapter includes a direct memory access controller for controlling transfers of said data between said interface adapter and said buffer memory (Column 11 lines 38-44 of Berry).

As per dependent claim **38**, the combination of Berry and Kitamura teach,

   o   The storage controller of claim 35, wherein said buffer memory comprises said memory for storing said access table (Paragraph 0026 as shown in Figure 1 of Kitamura). *The Examiner notes that the memory of Kitamura is used for the frequent access of frequently accessed data. The table is accessed frequently. Thus the table can be stored in the memory for ease of accessing.*

As per independent claim **53**, the combination of Berry and Kitamura teach,

   o   A storage router for providing virtual local storage on remote storage devices to devices, comprising: a buffer providing memory work space for the storage router; (Paragraph 0026 of Kitamura).

   o   a first controller operable to connect to and interface with a first transport medium, operable to implement access controls for storage space on the storage devices; a second controller operable to connect to and interface

with a second transport medium; and (Column 3 lines 8-18 as shown in

Figures 1 and 2 of Berry). *The Examiner notes that Berry teach multiple*

controllers, thereby anticipating the instant limitation.

- o a supervisor unit coupled to the first controller, the second controller and

    the buffer, the supervisor unit operable to map between devices

    connected to the first transport medium and the storage devices and to

    process data in the buffer to interface between the first controller and the

    second controller to allow access from devices connected to the first

    transport medium to the storage devices using native low level, block

    protocols (Column 7 lines 14-22 of Berry).

As per independent claim **71**, the combination of Berry and Kitamura teach,

- o A storage router for providing virtual local storage on remote storage

    devices to devices, comprising: a buffer providing memory work space for

    the storage router; (Paragraph 0026 of Kitamura).

- o a first controller operable to connect to and interface with a first transport

    medium, operable to map between devices connected to the first transport

    medium and the storage devices; a second controller operable to connect

    to and interface with a second transport medium; and (Column 3 lines 8-

    18 as shown in Figures 1 and 2 of Berry). *The Examiner notes that Berry*

    teach multiple controllers, thereby anticipating the instant limitation.

- o a supervisor unit coupled to the first controller, the second controller and

    the buffer, the supervisor unit operable to implement access controls for

storage space on the storage devices and to process data in the buffer to

interface between the first controller and the second controller to allow

access from devices connected to the first transport medium to the

storage devices using native low level, block protocols (Column 7 lines 14-

22 of Berry).

Claims **13-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Berry and in view of Hubis et al (U.S. 6,343,324) hereinafter referred to as Hubis.

As per dependent claim **13**, Berry teach the limitations as noted supra.

Berry does not explicitly teach the use of RAID.

Hubis teach, the storage controller of claim 1, wherein said microprocessor

performing said processing requests comprises performing redundant array of

inexpensive disks (RAID) processing (Column 7 lines 37-38).

Berry and Hubis are analogous art because they are from the same field of

endeavor, namely computer storage systems.

At the time of invention it would have been obvious to one of ordinary skill in the

art, having both the teachings of Berry and Hubis before him/her, to extend the

interfaces of Berry to encompass RAID systems for the benefit of increased

compatibility.

The motivation for doing so would have been that increased system capability

allows for additional systems that the Berry system is employed upon. Increasing the

number of interfacing standards also allows more flexibility when selecting the

components to comprise the system.

Therefore, it would have been obvious to combine Berry with Hubis for the benefit of increased capability to obtain the invention as specified in claims 13-23.

As per dependent claim **14**, Hubis teach,

- o The storage controller of claim 1, wherein said plurality of logical storage devices comprise one or more physical storage devices (Column 7 lines 39-46).

As per dependent claim **15**, Hubis teach,

- o The storage controller of claim 1, wherein said plurality of logical storage devices comprise one or more disk storage devices (Column 7 lines 39-46).

As per dependent claim **16**, Hubis teach,

- o The storage controller of claim 1, wherein said plurality of logical storage devices comprise one or more CDROM storage devices (Column 7 lines 39-46).

As per dependent claim **17**, Hubis teach,

- o The storage controller of claim 1, wherein said plurality of logical storage devices comprise one or more tape storage devices (Column 7 lines 39-46).

As per dependent claim **18**, Hubis teach,

- o The storage controller of claim 1, further comprising: a plurality of said microprocessors, coupled to said host interface adapter and said device interface adapter, wherein said host interface adapter determines which

one of said plurality of microprocessors is configured to process requests

for said logical storage device identified in said request and provides said

request to said determined one of said plurality of microprocessors (Figure

2A shown as the individual fibre channel processors).

As per dependent claim **19**, Hubis teach,

o The storage controller of claim 1, wherein each of said requests specifies

one of said plurality of host computers based on a unique world wide

name (Column 4 lines 49-53).

As per dependent claim **20**, Hubis teach,

o The storage controller of claim 1, wherein each of said requests specifies

one of said plurality of host computers based on an internet protocol

address (Column 7 lines 19-21).

As per dependent claim **21**, Hubis teach,

o The storage controller of claim 1, wherein each of said requests specifies

one of said plurality of host computers based on an identifier in a SCSI

request (Column 7 line 14).

As per dependent claim **22**, Hubis teach,

o The storage controller of claim 1, wherein each of said requests specifies

one of said plurality of logical storage devices in a protocol-specific

manner (Column 7 lines 10-14).

As per dependent claim **23**, Hubis teach,

o The storage controller of claim 22, wherein said protocol-specific manner

comprises an identifier in a SCSI request (Column 7 line 14).

Response to Arguments

Applicant's arguments, filed 3 October 2006, have been fully considered and are

persuasive. However, upon further consideration, a new ground(s) of rejection is made

as shown *supra*. Accordingly, this action has NOT been made final.

Conclusion

The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure.

1. U.S. 7,107,359 Burton et al teach a host-fabric adapter that offloads access

control from the microprocessor at least as shown in the abstract.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Matthew Bradley whose telephone number is (571) 272-

8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BRP/mb
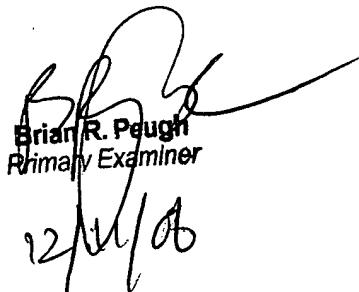
Brian R. Peugh
Primary Examiner

12/14/06